Under the Industrial PhD Programme (IPP) framework initiated by Economic Development Board Singapore, TUM Asia and Lantiq Asia Pacific Pte Ltd have partnered to embark on the following research project. This project aims to also provide postgraduate training in a corporate research and development environment where suitable candidates will be offered opportunities to conduct research and pursue PhD conferred by TUM with support from the Singapore government.

Details of the programme:

Duration: 4 years (no bonds required after the completion of the project)

Remuneration: Up to SGD3,300 (neg) per month with CPF contribution and AWS

Application Criteria: Singaporeans and PRs ONLY.
Minimum education qualification – Master degrees holder

Supervising Professor: Prof. Andreas Herkersdorf (Chair of the Integrated Systems Laboratory,TUM)

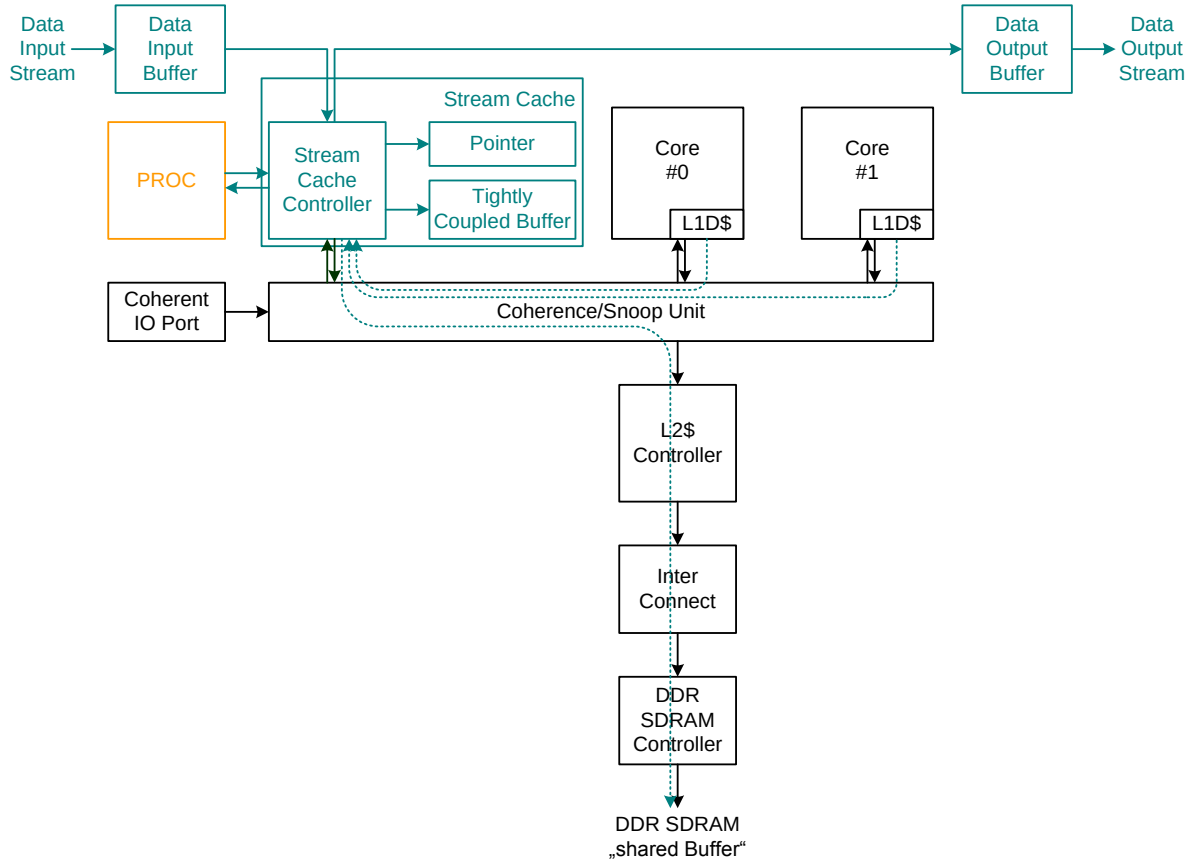
Company attached to: Lantiq Asia Pacific Pte Ltd http://www.lantiq.com/

Project Title: Cache Cohorent Accelerator Engine including Stream Cache

Abstract

A Coherent Processing System (CPS) is a cluster of processors interconnected to enable cache coherence in the primary data caches (L1D$). Each CPU core participating in the coherent system may access data structures, variables etc. in a cached and coherent way. This eliminates data copy operations between CPU cores as well as reduces stall cycles caused by these copy operations.

Standard multi-core CPU systems offered by IP providers like MIPS and ARM implement such Coherent Processing Systems e.g. MIPS 1004K. Furthermore, these CPS provide a coherent input port, which is designed to connect Accelerator Engine(s). These tightly coupled Engines take care of special tasks e.g. CRC checksum calculation, offloading the main CPU(s). These Engines deal with a subset of the workload in processing and controlling a data stream e.g. low level tasks. The upper layers of the software stack have to be processed by the main CPU(s). An Acceleration Engine may be comprised of an optimized hardware state machine, a programmable and deeply embedded CPU, or a combination of both. Data streams are received via high speed interfaces like Ethernet, PCIe, etc… optionally pre-processed by Accelerator Engines, processed by the main CPU(s), and forwarded to be transmitted via the high speed interfaces. Note, that such standard multi-core CPU systems do not foresee Accelerator Engine(s) to be directly connected to the Coherence Manger or Snoop Unit.



The cache coherent Acceleration Engine including a stream cache is the logical next development step, connecting the Engine and its cache to the Coherence Manager. Data received via the high speed interfaces is filled into the stream cache and is therefore already residing in the coherent CPU cluster. The stream cache takes care that always the next to be processed data item e.g. Ethernet header is immediately accessible by the Acceleration Engine as well as the main CPUs.
In case the system can not process the input data stream at wire speed, the stream cache pushes data temporarily to main memory. This push and pop operation is handled autonomously by the stream cache, fully transparent to the CPU and Software.
The stream cache is optimized for sequential work on buffers. The target setting is similar to today's caches in the sense that it should minimize the number of stall cycles required to fetch data. While today's cache algorithms make only heuristic assumptions deciding which data is evicted from the cache, the stream cache makes use of the fact that the application's buffers are handled sequentially. The initial step is to define a steam cache including appropriate cache algorithm. Additionally, a simple acceleration engine e.g. CRC check is required, which will be connected to the stream cache. Proof of concept is performed, emulating these units in Software e.g. running on a MIPS CPU core. Second, the stream cache and acceleration engine are implemented and tested on a hardware emulator. The final step adds "coherency" i.e. the steam cache including the accelerator engine is connected to the Coherence Manager of a Coherent Processing System.

At the end of the project, upon submission of his/her PhD thesis and successful defence of his/her thesis, the candidate will be conferred his/her post-doctorate by TUM.

Interested applicants, kindly submit your latest resume to gary.ong@tum-asia.edu.sg